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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,020	04/27/2005	Carl Glasse	GB02 0182 US	1660
24738 7590 12/19/2006 PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131			EXAMINER TAYLOR, EARL N	
			ART UNIT	PAPER NUMBER
			2818	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		12/19/2006	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/533,020

Applicant(s)

GLASSE ET AL.

Examiner

Earl N. Taylor

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 April 2005 to 4 February 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8, 10-12, 14-16, 18 and 19 is/are rejected.
- 7) ☒ Claim(s) 9, 13 and 17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>4/27/2005</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
- (e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
- (f) BACKGROUND OF THE INVENTION.
 - (1) Field of the Invention.
 - (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (g) BRIEF SUMMARY OF THE INVENTION.
- (h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
- (i) DETAILED DESCRIPTION OF THE INVENTION.
- (j) CLAIM OR CLAIMS (commencing on a separate sheet).
- (k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
- (l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Objections

Claims 2-6 and 8-17 are objected to because of the following informalities:

- Claims 2-6 recite "A TFT" in the preamble and should read --The TFT--.

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- Claims 8-17 recite "A method" in the preamble and should read --The method--.
- Claim 9 recites "according to claim 9" in the preamble and should read --
according to claim 8-- based on the antecedent basis of the claimed limitations.
- Claim 17 does not appear to end with proper punctuation.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 18 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite in that it fails to point out what is included or excluded by the claim language.** These claims are omnibus type claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-4, 6-8, 10-12 and 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Takehashi et al. (PCT Publication No. WO00/54339). The**

English equivalent, Takehashi et al. (U.S. Patent 6,624,473 B1), is used hereinafter.

Referring to Claim 1, Takehashi teaches, in Fig. 3, a TFT comprising a polycrystalline silicon channel (170) extending between a source (150) and drain (160), a gate (4) overlying the channel, and of a thickness to define an upstanding gate sidewall, an LDD region (152, 162), and a spacer (414, 4141) overlying the LDD region (152, 162), wherein the spacer (414, 4141) comprises a conductive region that both overlies the LDD region (152, 162) and extends along the upstanding gate (4) sidewall.

Referring to Claim 2, Takehashi teaches all of the limitations of Claim 1 wherein the conductive region (414, 4141) comprises a layer that is thinner than the thickness of the gate (4) and has a first portion (4141) overlying the LDD region and a second portion (414) extending along the upstanding side wall of the gate (4).

Referring to Claim 3, Takehashi teaches all of the limitations of Claims 1 and 2 wherein the conductive region (414) comprises a layer of conductive material (metal).

Referring to Claim 4, Takehashi teaches all of the limitations of Claims 1-3 wherein the layer is a metallic layer. The language, term, or phrase "metallic layer deposited by sputtering", is directed towards the process of sputtering. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, *per se*, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In*

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re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference.

As such, the language "metallic layer deposited by sputtering" only requires the layer to be a metallic layer, which does not distinguish the invention from Takehashi, who teaches the structure as claimed.

Referring to Claim 6, Takehashi teaches all of the limitations of Claims 1 and 2 including a fillet (3) over the first portion (4141) of the conductive region. The manner in which the claim is written does not structurally define a fillet that distinguishes over the prior art. Therefore the element as taught by Takehashi meets the claimed limitation.

Referring to Claim 7, Takehashi teaches, in Fig. 12 and 13, a method of fabricating a polycrystalline silicon channel TFT with a gate overlying the channel, having an upstanding gate side wall, the method comprising the steps of:

(a) providing a gate (42) separated from a polycrystalline silicon layer (1) by an insulating layer (2) (Fig. 12; steps a-f; Col. 19, Lines 34-62);

(b) implanting a dopant into the polycrystalline silicon layer (1) using the gate (42) as a mask (Fig. 12; step g; Col. 19, Line 63 to Col. 20, Line 5);

(c) forming a spacer (43) after step (b) adjacent to the gate (42) that comprises a conductive region which overlies the polycrystalline silicon layer (1) and extends along the gate (42) side wall (Fig. 12, step h to Fig. 13 step I; Col. 20, Lines 6-16); and

(d) implanting a dopant into the polycrystalline silicon layer (1) using the gate (42) and the spacer (43) as a mask to form a source or drain region (step j), such that the spacer (43) overlies an LDD region in the polycrystalline silicon layer (1) between the source or drain region and the channel (Col. 20, Lines 17-50).

Referring to Claim 8, Takehashi teaches all of the limitations of Claim 7 wherein step (c) comprises depositing a layer of conductive material (430) over the polycrystalline silicon layer (1) and the gate (42) (Fig. 12, step h; Col. 20, Lines 6-16), and selectively etching the deposited layer of conductive material (430) to form the spacer (43) with a first portion overlying the polycrystalline silicon layer (1) and a second portion extending along on the side wall of the gate (Fig. 13 step I; Col. 7, Lines 20-27 and Col. 8, Lines 35-38).

Referring to Claim 10 and 11, Takehashi teaches all of the limitations of Claims 7 and 8 including depositing the conductive material in a non-conformal layer and including depositing the layer by sputtering (Col. 15, Line 4; Col. 23, Lines 27-29). Wherein the specification defines a standard non-conformal technique to be sputtering (par. 33). Therefore because Takehashi teaches forming this layer by sputtering, the layer is defined to be a non-conformal layer.

Referring to Claim 12, Takehashi teaches all of the limitations of Claims 7 and 8 including depositing said layer as a metallic layer (Col. 20, Lines 6-16).

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Referring to Claim 14, Takehashi teaches all of the limitations of Claims 7, 8 and 11 including depositing a further layer (3) on said conductive layer (43), and selectively etching the further layer (step I) to form the fillet therefrom. The manner in which the claim is written does not structurally define a fillet that distinguishes over the prior art. Therefore the element as taught by Takehashi meets the claimed limitation.

Referring to Claim 15, Takehashi teaches all of the limitations of Claims 7, 8, 11 and 14 including depositing the further layer (3) as a conformal layer as the further layer conforms to the conductive layer (43).

Referring to Claim 16, Takehashi teaches all of the limitations of Claims 7, 8, 11 and 14 including depositing the further layer as a Si containing layer (Col. 20, Line 51).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takehashi.**

Referring to Claim 5, Takehashi teaches all of the limitations of Claims 1-3 but does not explicitly teach wherein the layer comprises a doped semiconductor material. However, it is notoriously well known that doped polysilicon is functionally equivalent to

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a metal. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a doped polysilicon layer as the conductive layer instead of a metal layer as taught by Takehashi because this would allow for greater and more precise control of conductivity and resistance of the gate electrode.

Allowable Subject Matter

8. Claims 9, 13 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims; And to overcome any other outstanding objections.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 9, the prior art of record alone or in combination neither teaches nor makes obvious the invention including depositing the layer of conductive material to a thickness, which is less than that of the gate in combination with all of the limitations of Claims 7 and 8.

Regarding Claim 13, the prior art of record alone or in combination neither teaches nor makes obvious the invention wherein the selective etching of the conductive layer is carried out by forming a fillet over the first portion thereof, and selectively etching the layer where not protected by the fillet in combination with all of the limitations of Claims 7 and 8. Claim 17 includes all of the limitations of Claim 13.

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Telephone / Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Earl N. Taylor whose telephone number is (571) 272-8894. The examiner can normally be reached on Monday-Friday from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MinSun Harvey can be reached on (571) 272-1835. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: Earl N. Taylor

Andy Hough
Andy Hough
Primary Examiner